Method and apparatus for producing test model f circuit block capable of reducing loa and time

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Inventor: SHIGEKAZU OTSUKA (JP)
Applicant: NIPPON ELECTRIC CO (JP)
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In a method for generating a test pattern for testing at least one circuit block (24-1, 24-2, 24-3) of a semiconductor device including a control circuit (21) connected to the circuit block the above-mentioned test pattern is generated by converting a common test pattern (11) for the circuit block with reference to a data conversion library (12) corresponding to characteristics of the control circuit.

Fig. 1